

Improving Nanoelectronic Designs Using a Statistical Approach to Identify Key Parameters in Circuit Level SEU Simulations

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Abstract—One of the key challenges in nanoelectronics design is the decreasing reliability due to radiation induced single-event upsets. Without detailed device level simulations or physical experimentation, circuit level models can generate misleading reliability information. We present the results from a screening experiment to identify significant parameters in circuit level SEU simulations. We show that cell supply voltage, sizing parameters, and transient waveform descriptions have an important impact on design and should therefore be considered with care in circuit level designs. Larger variations in parameters can lead to soft error rate estimates that vary by more than 4 orders of magnitude, even small variations can lead to 15x variation in soft error rate estimation for a design. We present our methodology for screening and a ranking based on significance of several parameters involved in soft error simulation at the SPICE level. *Index Terms* — circuit level reliability, single event upset (SEU), soft-error rate (SER), Plackett and Burman design, Q_{crit}

I. INTRODUCTION

Research is increasingly focused on the growing soft error rates (SERs) in CMOS and the related reliability problems [7], [8], [43]. Soft errors arise due to a higher susceptibility to alpha and neutron radiation [11], [35], [55]. The problem of dealing with these errors has traditionally been a problem for memory designers, however research indicates that within the next decade the problem of soft errors could be as great in logic as it is in memory now and therefore is becoming significant for circuit designers and computer architects [43].

A large number of analytical and simulation methods have been described to give designers tools necessary to assess the impact that radiation based effects will have on designs [1], [10], [15], [21], [36], [44], [50], [51]. Often times these models relying on extracting or estimating key parameters from a design or cell library in order to estimate the soft error rate (SER) for a given design, such as critical charge, Q_{crit} , or pulse width. When variations in critical parameters are not considered, larger errors can be introduced into these estimations.

The goal of this paper is to highlight significant parameters for the designer who may not have access to the detailed device models, such as academics working on fault-tolerance solutions, that are required to calibrate circuit level simulations.

The knowledge of which parameters can be safely estimated and which must be carefully considered can save a great deal of time.

In our investigation, we utilize statistical screening methods to identify key parameters involved in circuit level simulations of SEUs using HSPICE. We show that certain parameters, such as V_{DD} , W_{min}/L_{min} , and W_p/W_n , must be considered carefully by the designer due to their significant impact on the estimates of SER. Estimated SER can vary by more than 4 orders of magnitude if parameters are not chosen carefully, due to the exponential dependence on Q_{crit} . With as little as 10% variation in key parameters, Q_{crit} for a cell can vary by more than 70% and lead to a difference in SER estimates of more than 15x.

We will begin with a short description of the soft error mechanisms and how it relates to circuit level simulation. We then describe the screening design method we have chosen to employ for this investigation. The description of the simulation methodology is then presented and followed by a selection of collected data and results. Finally we conclude with a description of related works, discussion of challenges to experiments of this type, importance of these results to the designer and architect, and conclude with a brief summary.

II. SOFT ERROR OVERVIEW

This section briefly states the mechanisms behind SEU generation and how it relates to circuit-level simulation, however, a complete discussion of the mechanisms of SEUs is beyond the scope of this paper and we refer the reader to [3], [11].

For this paper we will consider only radiation sources of SEUs. The two primary types of radiation causing SEUs are alpha particles from packaging and device materials, and neutrons originating from cosmic rays. When an energetic particle strikes in a sensitive area, such as the area near the reverse biased drain junction in a transistor, electron-hole pairs are generated. The electrical field will then separate the holes and electrons and create a current. If the induced current is sufficient, the logical state of the transistor can be changed. This is then what we call a single event upset. If the SEU

signal propagates to a circuit output, it is then considered a soft error.

Modeling SEUs at the circuit level is commonly achieved using a current source at the site of proposed impact and a measurement of Q_{crit} , and possibly other information such as width, is made [11], [33], [46]. The critical charge, Q_{crit} , is then defined as a charge capable of generating an erroneous output signal sufficiently large enough to be latched or in some other way observed beyond the impact site. In section IV and section V more details are provided about the specific implementation of this method.

Finally, the definition of SER is simply the rate at which errors occur due to SEUs. The units are usually in errors per second, but it is often times declared in terms of bits or other design related quantities.

III. SCREENING

The purpose behind using a screening experiment is to identify and estimate the effect of key factors impacting some result, such as Q_{crit} . In this case, we wanted to examine the impact that several simulation parameters have on the measurement of Q_{crit} ¹ for various CMOS logical cells using HSPICE simulations.

Using such a rigorous statistical technique can:

- Identify where errors in Q_{crit} , SEU, and SER measurements are likely to occur in simulations. This is useful for architects and designers who need to quickly identify sources of errors in simulation results.
- Statistically support results based on careful parameter selection. Fault tolerance designers can be more sure of simulations demonstrating the impact of their designs on soft errors; architects can be more confident in the reliability estimates for designs.
- Reveal additional properties of Q_{crit} measurements at the circuit level.

There are several statistical techniques available to us. The choice to use a Plackett-Burman (PB) design was chosen due to the ability to examine 11 factors in 12 runs [37]. Other models considered were “one-at-a-time” (OAT) (varying one parameter at a time and noting the effects), exhaustive (examining all 2^N possible parameter combinations), and fractional geometric 2^{k-p} designs (examining corner cases for the parameters and requiring $\frac{1}{k-p}2^N$ runs). The reasons for not using these other methods were that they either did not provide enough information or required additional costly runs.

A. Summary of the method

The PB design describes a method for varying up to N-1 parameters simultaneously over N trials to estimate the effects on the outcome the parameters have. The main effects, parameters, are aliased with 2-factor and higher factor effects. For example, if we were to consider the effect on Q_{crit} had by the operating voltage (V_{DD}), the effect may not be that of V_{DD} , but rather the combined effect of temperature and fanout

due to aliasing. We would say that V_{DD} , a main effect, is aliased with temperature-fanout, a 2-factor interaction effect. It would also be aliased with additional 3-factor and higher effects as well, which are typically neglected.

An improvement on the PB design is the PB design with “fold over” (PBwFO)[25], [29]. This method breaks the aliasing chain between the main effects and the 2 factor interaction effects. The cost of this improvement is a doubling of the number of trials required from N to 2N. This is still, generally, a lower number of runs than a comparable resolution IV fractional geometric design. Also, other significant higher order interactions may still exist. We will assume that these interactions are not significant for this investigation.

To simulate an experiment based on the PBwFO design we construct a design matrix. A design matrix consisting of “+1” and “-1” is used to determine values for each parameter in a given trial. The value “+1” corresponds to a high value for the parameter and “-1” corresponds to a low value. The columns correspond to the individual parameter values for a given trial and the rows describe the state of all parameters for a given trial. Each experiment will then have 2N trials.

The first row of the matrix is taken from [37]. The next N-2 rows are constructed by shifting the previous row one place to the right and placing the final column value in the first column of the new row. The N^{th} row is constructed by placing all “-1” values in it. The bottom half of the matrix is created by inverting the values of the top half; if the value on the top half of the matrix is +1 it will be -1 on the bottom and vice versa.

The determination of high and low values can be set by using an OAT method. High values are those that increase Q_{crit} and low values the opposite.

First, we measure the result for each trial, such as Q_{crit} . To find the estimated effect for a given parameter, we multiply the result, Q_{crit} , of each run by the corresponding column value for the parameter, +1 or -1. We then sum all of the values and multiply by a factor given in [29]. For example, an effect might be estimated by :

$$Eff = \alpha(1*Q_{crit,1}) + (-1*Q_{crit,2}) + \dots + (1*Q_{crit,N}). \quad (1)$$

This yields the estimated effect that a given parameter has on the result. The magnitude of the estimated effect then reveals the significance of the parameter, the sign of the effect is not meaningful.

B. Cautions

There are dangers when using a non-geometric PB design, as has been noted in [30]. The main problem with non-geometric PB designs is the ambiguity of results. Main factor effects may be mistakenly identified instead of 2-factor interactions effects, due to aliasing. Additionally, significant 2-factor interactions may be missed. The use of the PBwFO design ensures that all main effects are identified but does not ensure that effects from any higher factors are shown.

To determine whether any 2-factor interacts were significant we examined several cells using the 32 trial 2_{IV}^{11-6} geometric

¹A discussion of the choice to use Q_{crit} is presented in section VII.

design. In the geometric design we found no effects of primary significance, but several of secondary significance. This does not ensure that there are no 3-factor or higher interactions, but we assume that there are none.

Additionally, we compared the results from the geometric design to the PB design. We found similar effect estimates for the main effects; we use this as evidence for the sufficiency of the PB design.

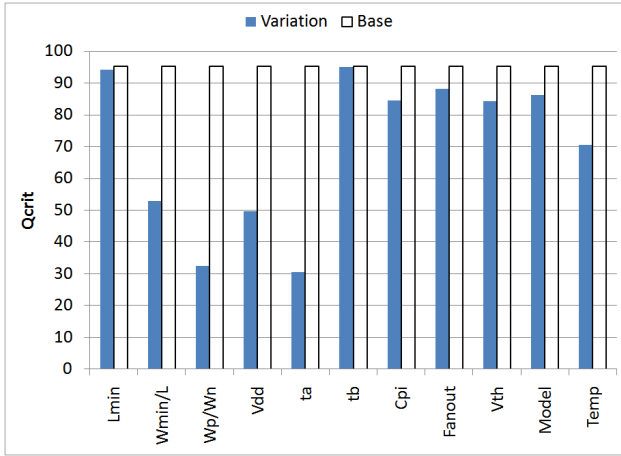


Fig. 1. In this figure we see the one-at-a-time results for the static INV cell. It shows the the drastic impact that individual parameters can have on Q_{crit} , while others have relatively little impact.

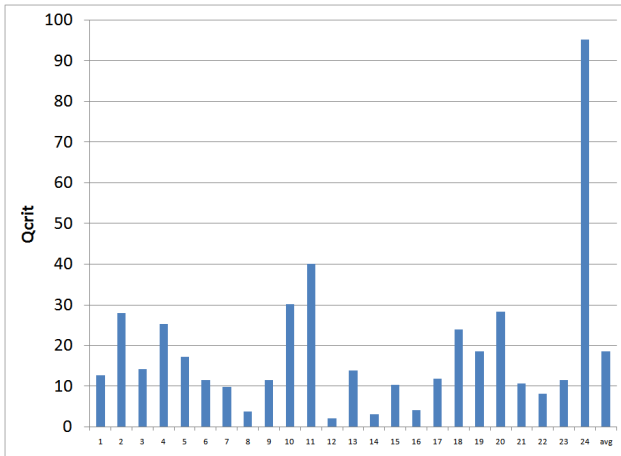


Fig. 2. Here we see the variation in Q_{crit} across a number of trials for the INV cell using the large variation of parameters design in the Plackett and Burman with Fold Over design. Each bar represents 1 run with the average Q_{crit} across all runs included as the last bar on the graph.

IV. SELECTION OF PARAMETERS

The importance of physical testing, such as accelerated radiation testing, or detailed physical simulators in calibrating circuit level simulation have been noted [40], [41], [46]. However, this option may not be available to designers for any number of reasons: cost, complexity, use of proprietary libraries, lack of particle accelerators. Our goal for this paper is to identify critical parameters necessary for accurate

SEU modeling at the circuit level. For designers who need accurate SER estimates, these parameters can identify where time should be spent locating characterization details and reduce additional costs and time. This information can also be valuable for the many methods of estimating SER using SPICE only for certain aspects of characterization such as [15], [50].

Other works have identified a number of critical and key parameters necessary for the characterization of SEUs. However, these can sometimes be vague or contradictory, as in the case of the importance of pulse shape, a parameter considered unimportant by some [10], [18], [23] and considered critical by others [4], [44], [48].

Most papers that discuss the effect of a variation in parameters have on SEU typically use an OAT approach. Examples include variation in Q_{crit} [19] or pulse width [10] where individual parameters are checked locally for effect on Q_{crit} or pulse width. These results are helpful in identifying which parameters to consider more thoroughly through detailed modeling or characterization but lack important information that cannot be obtained in OAT experiments, such as parameter interaction or averaging across other parameter levels. These experiments often times are highly dependent on the selection of the base case and yield less confidence in results than using PB type designs and can be misleading.

Other studies include the error that can be generated from variation or error in parameters. It was, for example, shown that small errors (15%) in transient pulse estimation can lead to very large (52%) errors in SER estimation even in very small circuits [48]. Further, process corner variations can alter SEU pulse widths by up to 75% [31]. It has also been shown that 34% error in pulse width estimation can occur after as few as 3 NAND2 gates [4]. Other papers of note include [23] for its discussion of using a current threshold rather than Q_{crit} in SPICE simulations and [34] for its discussion of soft error mechanisms and silicon process impact on SER.

The next subsection discusses several additional related works. Many of these works have stated the importance of some parameters, as described below, but very few –as noted above– have attempted to rank or even estimate their effects on SEU simulation when considered together. Our contribution is to bring together a large number of these parameters and rank their importance on circuit level simulation.

A. Parameters

It is a common practice to characterize a technology or design using device level simulations and then use SPICE, or one of its variants, to determine Q_{crit} in order to determine reliability [15], [50], [46]. There are a variety of parameters that go into determining Q_{crit} . In this section, we identify those parameters cited in the literature related to Q_{crit} simulations.

We have grouped identified parameters into larger categories. Those categories are: voltages, sizing parameters, current injection models, capacitances, and environmental factors. Within these parameters several sub-parameters are identified and examined.

We begin with cell operating voltage, V_{DD} . This parameter has been identified as a critical parameter in nearly all previous studies. As V_{DD} continues to scale downward, the Q_{crit} correspondingly decreases with an approximate relationship of $Q = CV$, where Q corresponds to Q_{crit} , C represents the nodal capacitance, and $V = V_{DD}$. The scaling trends for V_{DD} can be seen in [42].

The second member of the voltages category is threshold voltage, V_{th} . Threshold voltage for a cell has been identified due to its impact on leakage current and consequently on SEU and Q_{crit} [6], [10], [14], [19], [39]. Increasing V_{th} results in slower cell, which results in longer SEU pulses that are more likely to be latched. However, increased V_{th} also results in increased SEU attenuation [10].

After operating voltages, sizing is most often identified as a critical parameter. Typical models show that a node's SER is roughly proportional to the diffusion area [34], [43]. It has also been suggested that SER has additional high order dependences on sensitive area that requires more careful consideration, beyond those normally considered in SER calculations [46]. Sizing parameters have a direct impact on the drive current and consequently on Q_{crit} . It has been suggested that this effect dominates the nodal capacitance effect on Q_{crit} , a parameter that dominates Q_{crit} for memory [5]

The following sizing parameters all have been identified in previous investigations: minimum channel length (L_{min}), minimum width to length ratio (W_{min}/L_{min}), PMOS width to NMOS width (W_p/W_n), minimum diffusion length (dif). These papers describe many of the significances of various sizing parameters, including Q_{crit} effects, [10], [16], [19], [28], [32], [44], [46], [54].

Sizing is also of great interest to us due to the increasing number of fault-tolerance methods utilizing cell re-sizing to address the soft error problem [2], [5], [6], [27], [51], [53].

As noted above, nodal capacitance dominates Q_{crit} in memory. Nodal capacitance in logic is due to three factors: cell capacitance, parasitics, and load. The nodal capacitance at the site of the particle strike determines either how much charge must be built up or dissipated. Nodal capacitance can be thought of as a function of fanout and scaling; smaller device geometries result in smaller nodal capacitances. It is shown to have a significant effect on SER in a large number of studies, due to the effect loading has on both the shape and amplitude of SEU induced pulses [28], [31], [38], [46], [48], [50].

The layout of the cell, as well as the materials used, determine the cell capacitance. Load is determined by the number of cells that are connected to a given node and is often modeled by equivalent capacitors or fanout in circuit simulations.

Parasitic capacitance arise due to wiring and other sources. Process variations can also lead to differences in parasitic and gate capacitances. Parasitic capacitance has been considered and shown to have some effect on Q_{crit} in 65nm SOI [19].

In addition to circuit and device considerations, we also consider the current source models used by various researchers.

The modeling of the particle strikes is done using an ideal current source, as is standard practice for circuit level simulations [11], [33], [46]. The particular waveform shape used is considered important by some [44] and unimportant by others [10], [18], [23].

There are two categories of models for current injection: abstract and fits. Abstract often try only to capture one or two characteristics of the current pulse, such as width and amplitude. The other category of current pulse models use either single or double exponential curves fit to device level data.

The abstract models include current pulses modeled as: triangular [22], [23], rectangular [23], [40], gaussian [23], [40] and trapezoidal waveforms [10], [27], [36].

A double exponential model for current injected as a result of a SEU is presented in [24], equation 2. An additional single exponential current model is presented in [13], and is described in 3. The exponential models have also been approximated using piecewise linear methods [21], piecewise quadratic methods [9], and using a 3-parameter Weibull model [38]. It has been stated that the model of [13] can be exchanged with that of [24] without loss of generality [6]. In equation 2, Q is the injected charge, t is time, t_α is the charge collection constant, and t_β is the ion track establishment time. The additional parameter in equation 3, τ , is a collection time constant parameter.

$$I_1(t) = \frac{Q}{t_\alpha - t_\beta} (e^{-t/t_\alpha} - e^{-t/t_\beta}) \quad (2)$$

$$I_2(t) = \frac{2Q}{\tau\sqrt{\pi}} \sqrt{\frac{t}{\tau}} e^{-t/\tau} \quad (3)$$

We chose to use the two exponential waveforms for our current models in this investigation. The error introduced due to other models, such as the trapezoidal method, have been discussed elsewhere [4], [47], [48].

The two important parameters in equation 2, aside from charge (Q), are t_α and t_β . The collection time constant of the junction, t_α , is a technology dependent parameter. In many investigations t_α is based on technology characterization through physical experimentation or device level simulation [19], [46]. Many other investigations rely upon published information or variable values [14], [53]. Values for t_α range from 10s of picoseconds [6] to 100s of picoseconds [18], [54], but are typically in the range of 50-100 ps for (bulk) technologies in the 65nm scale. Trends in the scaling of collection time constants can be found in [16].

The second technology dependent parameter of equation 2 is the ion track establishment time, t_β . This is also called the rise time in a number of papers. Values for t_β range from less than a picosecond [19] to 10s of picoseconds [9], [54]. The typical value for t_β is $< 10^{-11}$ s. It is generally considered a less important parameter than the collection time constant [19], [44].

In [6] the authors comment that the single and double exponential waveforms can be interchanged without loss of generality.

We will consider the two parameters from equation 2 and an approximation to the single parameter from 3.

To find the closest match between $I_1(t)$ and $I_2(t)$ we evaluated both equations over the variation values of t_α

$$\tau \approx -0.0008(t_\beta)^2 + 1.0552t_\beta + .562t_\alpha - 0.0774. \quad (4)$$

We use this to approximate τ according to the varying t_α and t_β values. Trends in the scaling of τ can be found in [16].

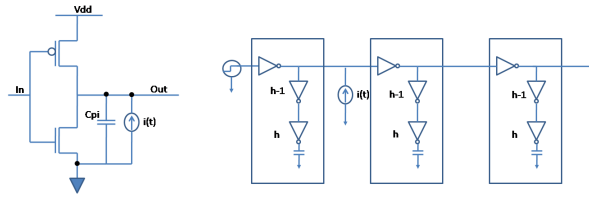
Finally, the last parameter category that we will consider is operating conditions. The main significant environmental parameter that we identified is temperature. Temperature is considered due to the effect that it has on mobility and carrier concentrations which in turn affect Q_{crit} . Higher temperatures have previously been shown to lower Q_{crit} and increase SER[20].

V. SIMULATION

All measurements of Q_{crit} are from HSPICE simulations using the 65nm ptm technology models [52]. Changes to the model, such as V_{th} variation, were done according to methods described in [12]. All logic cells are generic static cells. Examined cells are listed on tables II - V.

Determination of Q_{crit} was made using the built in optimization function from HSPICE. The goal value of Q_{crit} was set at the point where the output signal from the cell reaches $V = V_{DD}/2$ [5], [49], [54].

Based on the works cited in section IV-A, high, low, and typical parameters were chosen for the simulations of 65nm technology, see table I.



(a) Example setup for current injection into a single INV cell.

(b) Chained cells with fanout h. model

Fig. 3. In (a) we see the general model for injecting current pulses. In (b) we see the model for injecting current into a chain of INV cells with capacitive loads generated using fanout.

A. Large and Small Variation

We have generated two cases for examination. The first case involves large variation of parameters, and the second utilizes smaller variations. We are interested in the impact and significance for each parameter related to Q_{crit} for large variations of parameters, such as in the case where information is lacking and parameters are estimated or guessed, and in the

TABLE I
PARAMETER CHOICES FOR EXPERIMENTS.

Parameter	10%		Large	
	high	low	high	low
L_{min} (λ)	1.8	2.2	2	4
W_{min}/L_{min}	2.2	1.8	4	2
W_p/W_n	2.2	1.8	4	1
V_{th} (V)	0.44	0.36	.42	.22
V_{DD} (V)	1.1	0.9	1.2	0.8
Current Model	$I_1(t)$	$I_2(t)$	$I_1(t)$	$I_2(t)$
t_α (ps)	110	90	100	10
t_β (ps)	0.9	1.1	0.5	5
C_{pi} (fF)	1.1	0.9	10	1
C_{load}	h=4	h=3	h=4	h=1
Temperature ($^{\circ}C$)	72	88	25	80

TABLE II
RANKING MAIN FACTORS WITH LARGE VARIATION FOR VARIOUS CELLS.

Cell	L	W/L	P/N	Vdd	t_α	t_β	C_p	C_l	V_{th}	M	T
inv	10	4	1	3	2	11	6	7	8	9	5
nand2	10	4	1	3	2	11	6	7	8	9	5
nand3	10	4	1	3	2	11	6	7	8	9	5
nand4	7	4	1	3	2	11	5	8	9	10	6
nor2	6	5	1	3	2	11	4	7	9	10	8
nor3	6	5	1	2	4	10	3	7	9	11	8
nor4	7	5	1	3	2	10	6	4	9	8	11
xor2	6	4	1	2	3	10	5	7	9	11	8
xnor2	6	4	1	2	3	10	5	7	9	11	8
and2	9	4	1	3	2	11	5	7	8	10	6
and3	9	4	1	3	2	11	5	7	8	10	6
and4	9	4	3	2	1	11	5	7	8	10	6
or2	9	4	1	3	2	11	5	7	8	10	6
or3	9	4	1	3	2	11	5	7	8	10	6
or 4	9	5	1	3	2	11	4	7	8	10	6
avg	8.13	4.27	1.13	2.73	2.20	10.73	5.00	6.87	8.40	9.87	6.67
var	2.55	0.21	0.27	0.21	0.46	0.21	0.71	0.70	0.26	0.70	2.6

case where process variations due to manufacturing come into play.

The large variations are based on reported data and, when possible, taken from relevant (i.e. 65nm) technology processes. For example, collection time constants were reported from low 10s of ps to 100s of ps. We then take our large variation collection time constant, t_α , to vary from 10 to 100 ps.

The small variations are based on a fixed parameter value and varied by 10%, see table I. For example, we selected $V_{DD} = 1.0V$: $V_{DD}(+1) = 1.1V$, $V_{DD}(-1) = 0.9V$. Again, all parameter values were based on published information.

VI. RESULTS AND ANALYSIS

This section presents the results obtained from both the large and small variation of parameters.

For tables II–V, the following column headers are used: L = L_{min} , minimum channel length; W/L = W_{min}/L_{min} , minimum width to length ratio for transistors; P/N = W_p/W_n , ratio of PMOS transistor widths to NMOS widths; V_{DD} = supply voltage; t_α = junction charge collection time constant; t_β = ion track establishment time constant; $C_p = C_{pi}$, parasitic capacitance; $C_l = C_{load}$, capacitive load; V_{th} = threshold voltage; M = current injection model, single or double exponential; T = temperature.

TABLE III

ESTIMATION OF EFFECTS FOR THE MAIN EFFECTS USING LARGE VARIATION IN PARAMETERS FOR VARIOUS CELLS.

Cell	L	W/L	P/N	Vdd	t_{α}	t_{β}	C_p	C_l	V_{th}	M	T
inv	5.17	19.93	34.08	26.26	28.93	4.23	15.33	11.94	11.85	7.47	15.47
nand2	7.17	20.53	35.40	26.59	29.43	4.53	15.61	12.28	12.01	7.79	15.63
nand3	6.01	22.07	38.01	27.49	29.57	4.94	15.48	12.16	12.05	7.93	15.63
nand4	11.50	21.27	39.25	24.47	30.89	7.12	20.05	10.92	9.68	7.85	13.44
nor2	9.10	13.12	22.96	16.14	17.91	5.11	15.41	8.99	6.30	5.31	7.51
nor3	10.47	12.90	20.29	15.14	14.00	4.21	14.23	8.09	4.99	4.10	6.47
nor4	5.94	7.75	13.47	11.71	12.84	2.98	6.47	10.25	4.19	4.67	-1.91
xor2	12.87	16.51	25.77	18.85	18.56	5.74	16.18	11.76	7.08	5.65	8.51
xnor2	14.00	18.61	30.08	21.76	20.87	6.46	17.11	13.40	8.25	6.21	9.15
and2	8.51	19.13	33.09	25.83	29.42	4.31	15.91	12.53	12.10	7.73	15.73
and3	7.29	17.87	31.76	24.64	28.37	2.99	14.66	11.26	10.88	6.36	14.43
and4	7.68	22.47	22.86	28.97	34.80	3.97	16.08	12.83	12.02	7.65	15.01
or2	8.38	18.55	32.22	25.22	28.93	4.11	15.71	11.87	11.78	7.43	15.42
or3	8.18	18.33	31.94	24.97	28.65	3.98	15.56	11.59	11.57	7.27	15.23
or4	7.39	16.51	30.23	20.96	28.49	5.82	19.59	9.51	8.21	6.67	12.33
avg	8.64	17.70	29.43	22.60	25.44	4.70	15.56	11.29	9.53	6.67	11.87
var	6.52	15.54	49.85	25.57	45.24	1.39	8.92	2.22	7.91	1.55	25.41

TABLE IV

RANKING MAIN FACTORS WITH 10% VARIATION OF PARAMETERS FOR VARIOUS CELLS.

Cell	L	W/L	P/N	Vdd	t_{α}	t_{β}	C_p	C_l	V_{th}	M	T
inv	2	3	4	1	6	11	10	9	5	7	8
nand2	2	3	4	1	6	11	10	9	5	7	8
nand3	2	3	4	1	6	11	10	9	5	7	8
nand4	2	3	4	1	6	11	10	9	5	7	8
nor2	6	2	3	1	7	11	10	9	4	5	8
nor3	9	2	3	1	6	11	10	8	5	4	7
nor4	9	2	3	1	6	11	10	8	5	4	7
xor2	7	2	3	1	6	11	10	9	4	5	8
xnor2	5	2	4	1	7	11	10	9	3	6	8
avg	4.89	2.44	3.56	1.00	6.22	11.00	10.00	8.78	4.56	5.78	7.78
var	9.11	0.28	0.28	0.00	0.19	0.00	0.00	0.19	0.53	1.69	0.19

A. Results from the Wide Variation of Parameters

The data presented in table II shows the rankings for a variety of different cells for each of the varied parameters. A lower ranking would indicate a more significant parameter (i.e. the most significant factor has a ranking of 1 and the least significant has a ranking of 11). The magnitude of the effects are presented in table III. Parameter effect estimates we calculated according to methods used in [29], [30].

In figure 2, a variation of nearly 2 orders of magnitudes can be found for Q_{crit} , (2fC to 96fC). Using the SER equations from [43] with data extrapolated from [16], we find that this represents a variation in estimated SER of 10^4 x. This is an extreme case, but it demonstrates the necessity of careful parameter examination.

TABLE V

ESTIMATED EFFECT FOR MAIN FACTORS WITH 10% VARIATIONS OF PARAMETERS FOR VARIOUS CELLS

Cell	L	W/L	P/N	Vdd	t_{α}	t_{β}	C_p	C_l	V_{th}	M	T
inv	5.64	4.33	4.15	7.17	3.35	0.08	0.39	0.98	3.89	2.38	1.96
nand2	5.56	4.57	4.35	7.45	3.39	0.11	0.40	0.99	4.02	2.64	1.97
nand3	5.45	4.77	4.54	7.67	3.43	0.12	0.40	0.98	4.09	2.86	1.98
nand4	5.33	4.96	4.72	7.85	3.45	0.13	0.40	0.97	4.13	3.06	1.98
nor2	1.79	2.79	2.50	4.51	1.75	0.06	0.34	0.70	2.17	1.93	1.09
nor3	0.50	2.38	2.03	3.68	1.22	0.06	0.30	0.57	1.50	1.64	0.79
nor4	-0.31	2.24	1.84	3.31	0.97	0.06	0.28	0.50	1.08	1.44	0.64
xor2	1.62	3.28	2.77	5.09	1.83	0.08	0.33	1.05	2.39	2.20	1.12
xnor2	2.73	3.74	3.23	6.27	2.12	0.14	0.39	1.22	3.72	2.59	1.23
avg	1.89	2.20	2.01	3.53	1.43	0.06	0.21	0.53	1.80	1.38	0.85
var	5.79	4.09	3.60	10.73	2.06	0.00	0.03	0.23	3.15	1.54	0.69

B. Results from the Process Variation of Parameters

In addition to determining the impact that wide parameter variation will have on Q_{crit} measurements, we also wanted to determine the impact that $\pm 10\%$ of parameters would have.

The estimation of effects is given in table V, and the ranking of the most significant factors for each cell is given in table IV.

When values are unknown and could have large variations these parameters have the largest effect on Q_{crit} : W_p/W_n , V_{DD} , and t_{α} . Large variation in other parameters appears to have secondary effects on Q_{crit} and consequently SER. When variations are smaller, the effects were largest with: W_{min}/L_{min} , W_p/W_n , and V_{DD} . Secondary effect parameters include: L_{min} , V_{th} , t_{α} , the current model, and possibly temperature. Small variations in C_{pi} , t_{β} , C_{load} tended to have very small effect on Q_{crit} .

C. Analysis of Results

The advantage of using a PB design versus OAT methods is that PB captures the effect of interactions between parameters. Additionally, the effect of each parameter is averaged across the values of the other factors in the PB design, but is measured locally in OAT designs. Any contradiction between the effect a parameter is seen to have on Q_{crit} in OAT experiments versus this PB design may be related to either of these two issues.

An additional benefit to providing such information is that the rankings themselves can be incorporated into design methods. The cost of characterizing every individual cell in large designs is almost certainly too costly, but a summary of parameter impact could be used to improve future designs. For example, a designer may rely upon a table of parameter effect rankings to direct which cells are considered for fault-tolerance, rather than relying upon data for a single cell.

Finally, we could also use the single ‘‘worst case’’ values from the PB design to provide a bound for Q_{crit} . This would provide further confidence that the SER is conservative in its estimation. This approach has been criticized as overly pessimistic, in terms of SER estimation, however.

D. Additional Comments

In the wide variation experiments, we see a great deal of consistency in the rankings with nearly all parameters having a variance of less than one. The top three most important parameters are W_p/W_n , t_{α} , and V_{DD} . The rankings combined with the estimated effects seem to support the claim that drive current dominates nodal capacitance in Q_{crit} measurements [5]. Additionally, we see that several of the parameters have large variances in the estimated effects; a result expect due to the variation of Q_{crit} in various cells [48], and in contradiction to [26]. This emphasizes the danger of using equivalent INV cells to model other cells. Results are shown in tables II and III.

The impact of these parameters is highlighted for the INV cell with results for a OAT experiment shown in figure 1 and the PBwFO design in figure 2. It is interesting to see that figure 2 correctly identifies the top 4 significant parameters, but the

magnitude of change in Q_{crit} does not correctly correspond to the estimated effects or rankings.

Using the method of SER estimation from [43], we find that SER would vary more than 4 orders of magnitude for a circuit using Q_{crit} from the lowest ($\sim 2fC$) to highest values ($\sim 95fC$) based on this experiment, due to the exponential dependence on Q_{crit} .

When the parameter variations were confined to a narrower range, we see that V_{DD} and W_p/W_n are still dominant factors. However, t_a becomes less of a factor, and W_{min}/L_{min} becomes more significant. Results for ranking and effects can be seen in tables IV and V.

Even with only 10% variation in key parameters, Q_{crit} varies by more than 70% for the INV cell from its minimum value to its maximum value. A 200mV change in V_{DD} can result in more than a 20% change in Q_{crit} on its own.

VII. DISCUSSION

The first point that should be discussed is the decision to use Q_{crit} as the basis for our measurements. The metric Q_{crit} as the minimum charge necessary to generate a signal of amplitude $V_{DD}/2$ is a common one [5], [49], [54]. It does not, however, guarantee that the signal will propagate to a circuit output nor does it ensure the erroneous signal would be latched if it did propagate to an output [23]. If we were attempting to determine Q_{crit} for an actual design we would modify Q_{crit} to match the case where a signal is generated that is capable of being latched. Our choice to use Q_{crit} is based on its usefulness, accuracy, popularity and familiarity [33]. Additionally, it is a key item in SER estimation techniques [40], [43], [46]. For additional criticism of Q_{crit} as a metric see [11], [22].

In the future we plan to expand our metrics to consider critical pulse width, depth of propagation, and other related measurements to more fully characterize the critical parameters in circuit level simulations for SEUs. For discussion on issues involved with using pulse width as a SEU metric see [10], [47].

A. Discussion of Parameter Selection

The decision to include the parameters described was made based on the conclusions drawn by previous investigators. We examined a large number of related papers (many described below) and identified parameters previously declared to be paramount to SEU simulation.

We have also opted to consider only NMOS nodes. The reason for this was to limit the number of experiments. Based on previous work investigating SER estimates, we expect the results for PMOS to be similar to NMOS results for the other cells as well. Lastly, we chose to focus on NMOS due to the increased likelihood of NMOS SEUs [16]. However, we recognize the importance of characterizing both PMOS and NMOS based on results such as [17].

We also only considered output nodes, that is nodes with a drain junction connected directly to the output of the cell. This speeds up simulation time and also simplifies the injection model. Examining additional nodes in NAND and NOR cells

yielded very similar results, in terms of parameter ranking. As stated previously, input state can have a large impact on Q_{crit} , and for nodes not directly connected to the cell's output, this is especially true and should be considered for more accurate Q_{crit} measurements.

We have already begun to expand our investigation, for future publication, to include additional technology models, more nodes, additional logic cell layouts, actual circuit designs, and other SER related metrics, such as pulse width.

VIII. SUMMARY

In this paper we have presented a method for screening key parameters involved in circuit level simulations to determine Q_{crit} for individual nodes within cells. We have also demonstrated the impact that the variations in the choice of parameters can have on SER estimations based on these parameters. Simulations based on methods introducing even small error at the transistor level can result in large errors in SER estimates at the circuit level.

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