

# Guiding Circuit Level Fault-Tolerance Design with Statistical Methods

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## Abstract

*In the last decade, the focus of fault-tolerance methods has tended towards circuit level modifications, such as transistor resizing, and away from expensive system level redundancy approaches. We present the results from a screening experiment to identify significant parameters in circuit level soft error simulations to guide such approaches to fault-tolerance. This approach allows us to assess which parameters will have the most significance for reducing soft error rates and the impact that process variation will have on the accuracy of soft error rate estimates. We identify supply voltage and transistor type as being the most significant parameters affecting soft errors in logic cells across several technology scales. Additionally, we provide a ranking of more than a dozen parameters, across four technology scales, based on the significance of their impact on soft error rates.*

## 1 Introduction

Research is increasingly focused on the growing soft error rates (SERs) in CMOS and the related reliability problems [6, 27]. Soft errors arise due to a higher susceptibility to alpha and neutron radiation [3, 8]. The problem of dealing with these errors has traditionally been a problem for memory designers, however research indicates that soon, soft errors could be as great in logic as it is in memory now and therefore is becoming significant for circuit designers and computer architects [27].

Recently, a number of circuit level solutions and analysis methods have been proposed to address the SER issue in logic designs [1, 7, 11, 14]. Often times these methods rely on characterizing or estimating key technology parameters. The impact of process variations or error in parameter estimation is often not included or assumed to be small. It has been shown, however, that even small variation in key

parameters can lead to significant errors in SER estimation [30, 31].

The goal of this paper is, through the use of Plackett and Burman statistical screening methods, to provide meaningful information to designers looking to reduce soft error rates. This information serves three purposes, first to direct attention towards circuit level parameters that have the largest impact on soft errors, second to highlight critical parameters needed for SER estimation, and third to highlight the level of variation in  $Q_{crit}$  that can arise due to variation in these parameters.

## 2 Background

To find methods for reducing soft errors at the circuit level, a knowledge of the mechanisms responsible for errors is necessary. This often times requires detailed simulations. The importance of physical testing, such as accelerated radiation testing, or detailed physical simulators in calibrating circuit level simulation have been noted [25, 30]. However, this option may not be available to designers for any number of reasons: cost, complexity, use of proprietary libraries, lack of particle accelerators.

A number of critical and key parameters necessary for the characterization of soft errors have been identified in the past. However, these can sometimes be vague or contradictory, as in the case of the importance of pulse shape, a parameter which is considered unimportant by some [7] and considered critical by others[4].

Most papers presenting results discussing variation of parameters on soft errors typically show “one-at-a-time” type results. These experiments, often times, are highly dependent on the selection of the base case and yield far less precision than our chosen method and can be misleading. Examples of “one-at-a-time” analyses include variations of  $Q_{crit}$ [13] and pulse width [7]. These results can be helpful in identifying which parameters to consider more thor-

oughly through detailed modeling or characterization but lack important information.

Other studies include the error that can be generated from variation or error in parameters. It was, for example, shown that small errors (15%) in transient pulse estimation can lead to very large (52%) errors in SER estimation even in very small circuits [31]. Further, process corner variations can alter SEU pulse widths by up to 75% [19]. It has also been shown that 34% error in pulse width estimation can occur after as few as 3 NAND2 gates [4]. Other papers of note include [15] for its discussion of using a current threshold rather than  $Q_{crit}$  in SPICE simulations and [20] for its discussion of soft error mechanisms and silicon process impact on SER.

## 2.1 Contribution

Key parameters in device level simulations have been previously identified [25, 30]. Our paper highlights key parameters for circuit designers to target for error reduction and simultaneously demonstrates the sensitive nature of  $Q_{crit}$  to variation in parameters. We present a circuit level analysis ranking 14 parameters by significance of effect on  $Q_{crit}$ . We also consider 16 2-parameter combinations and their effects on  $Q_{crit}$ . Previous work assumes that either technologies can be readily characterized by device level simulation or experimentation or have examined parameter effects in single one-at-a-time type experiments.

## 3 Screening

The purpose behind using a screening experiment is to identify and estimate the effect of key factors impacting some result, such as  $Q_{crit}$ . In this case, we wanted to examine the impact that several parameters have on the measurement of  $Q_{crit}$  for various CMOS logical cells using HSPICE simulations.

Using such a rigorous statistical technique can:

- Identify where errors in  $Q_{crit}$ , SEU, and SER measurements are likely to occur in simulations. This is useful for architects and designers who need to quickly identify sources of errors in simulation results.
- Statistically support results based on careful parameter selection. Fault tolerance designers can be more sure of simulations demonstrating the impact of their designs on soft errors; architects can be more confident in the reliability estimates for designs.
- Reveal additional properties of  $Q_{crit}$  measurements at the circuit level.

We use a Plackett-Burman (PB) design method, chosen because of the ability to examine up to 15 factors/parameters in 16 runs [22]. Compared to “one-at-a-time” methods, PB methods yield more information, including parameter interactions and averaging of effects across a larger sample space. Exhaustive designs require  $2^N$  experiments. The PB design is compromise providing more information than “one-at-a-time” methods and, generally, far fewer trials than the exhaustive approach.

### 3.1 Summary of the method

The PB design describes a method for varying up to N-1 parameters simultaneously over N trials to estimate the effects on the outcome the parameters have. The 1-factor effects are aliased with 2-factor and higher factor effects. For example, if we examined the resulting effect operating voltage ( $V_{DD}$ ), had on  $Q_{crit}$ , we may not find the primary effect but the effect of a 2-factor effect, such as Temperature + fanout. We would say that  $V_{DD}$ , a main effect, is aliased with temperature+fanout, a 2-factor interaction effect. It would also be aliased with additional 3-factor and higher effects as well, which are typically neglected.

An improvement on the PB design is the PB design with “fold over” [18]. This method breaks the aliasing chain between the main effects and the 2 factor interaction effects. The cost of this improvement is a doubling of the number of trials required from N to 2N. Other significant higher order interactions may still exist, however, we will assume that these interactions are not significant for this investigation.

At the heart of the method is the design matrix. A design matrix consisting of “+1” and “-1” is used to determine values for each parameter in a given trial. The value “+1” corresponds to a high value for the parameter and “-1” corresponds to a low value. Each row in the matrix represents the values for all parameters in a single trial. The columns correspond to values for individual parameters over all trials.

The first row of the matrix is taken from [22]. The next N-2 rows are constructed by shifting the previous row one place to the right and placing the final column’s value in the first column of the new row. The  $N^{th}$  row is constructed by placing all “-1” values in it. The bottom half of the matrix is created by inverting the values of the top half; if the value on the top half of the matrix is +1 it will be -1 on the bottom and vice versa. Row  $N+1 = -1 \cdot (\text{Row } 1)$ , and so forth. Each experiment then has 2N trials corresponding to the 2N rows.

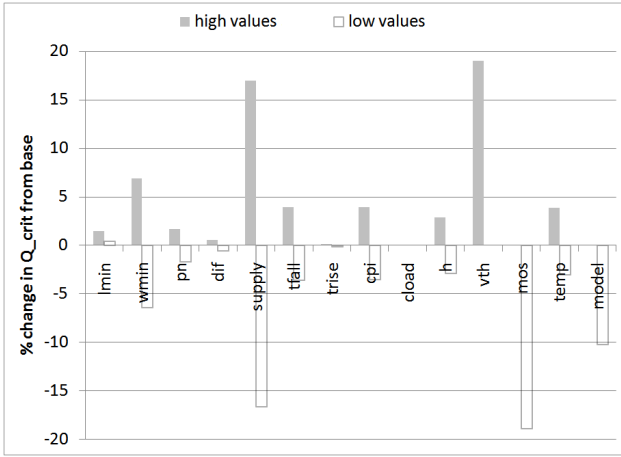
The determination of high and low values can be set by using a one-at-a-time method. We chose high values to represent parameters that increase  $Q_{crit}$ .

To estimate the effect we must measure a result for each trial. To find the estimated effect for a given parameter, we multiply the result, such as  $Q_{crit}$ , of each run (i), ( $Q_i$ )

by the corresponding geometric notation for the parameter,  $j = +1, -1$ . We then sum all of the values and multiply by a factor,  $\alpha$ , given in [18]. A parameter's effect is then estimated by :

$$\alpha ((j_1 * Q_1) + (j_2 * Q_2) + \dots + (j_N * Q_N)). \quad (1)$$

This yields the estimated effect that a given parameter has on the result. Two-factor effects are measured in a similar fashion but with two values of  $j$ . The magnitude of the estimated effect then reveals the significance of the parameter, the sign of the effect is not meaningful.



**Figure 1. In this figure we see the “one-at-a-time” results for the static INV cell (22nm).**

#### 4. Selection of Parameters

In this section, we identify and briefly discuss parameters cited in the literature related to  $Q_{crit}$  simulations.

$V_{DD}$  has a direct impact on the size of the charge necessary to generate a signal which can be propagated. Increases in cell threshold voltages,  $V_{th}$ , result in slower cells. Slower cells generate longer pulses that are more likely to latch SEUs. However SEUs are also more likely to be attenuated [7].

Typical models show that a node's SER is roughly proportional to the diffusion area [20, 27]. It has also been suggested that SER has additional high order dependencies on sensitive area [30]. Sizing also has a direct impact on the drive current and  $Q_{crit}$ . This effect dominates the nodal capacitance effect on  $Q_{crit}$  [5]. Particular sizing parameters identified in previous investigations include: minimum channel length ( $L_{min}$ ), minimum width to length ratio ( $W_{min}/L_{min}$ ), PMOS width to NMOS width ( $W_p/W_n$ ), minimum diffusion length (dif) [7, 12, 30, 34].

Nodal capacitance dictates  $Q_{crit}$  in memory but it is less clear for logic. We consider three aspects of capacitance in our investigation, parasitic capacitance  $C_{pi}$ , capacitance due to fanout, and capacitance due to end-of-circuit loading  $C_{load}$ . Capacitance has also been shown to have an effect on both the shape and amplitude of radiation induced pulses affecting  $Q_{crit}$  and SER [17, 19, 24].

Typically SEUs are modeled as an ideal current source in circuit level simulations [8, 21, 30]. We consider two models, a single and a double exponential waveform. The double exponential model is presented in [16], shown in equation 2. A single exponential current model is presented in [10], and is described in equation 3.

$$I_1(t) = \frac{Q}{t_\alpha - t_\beta} (e^{-t/t_\alpha} - e^{-t/t_\beta}) \quad (2)$$

$$I_2(t) = \frac{2Q}{\tau\sqrt{\pi}} \sqrt{\frac{t}{\tau}} e^{-t/\tau} \quad (3)$$

We also include the individual parameters from both waveforms,  $t_\alpha$ ,  $t_\beta$ , and  $\tau$ . Trends in the scaling of collection time constants can be found in [12].

The last parameter considered is temperature. Temperature is considered due to the effect that it has on mobility and carrier concentrations which in turn affect  $Q_{crit}$ .

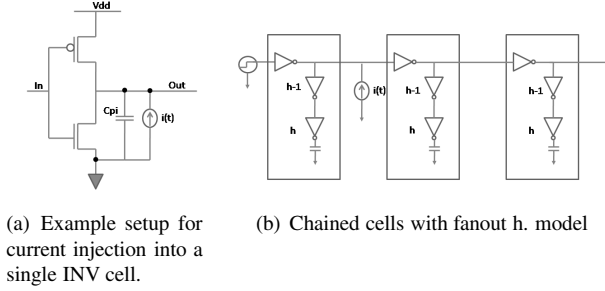
In total, we have identified and considered 14 parameters for their effect on  $Q_{crit}$ : supply voltage ( $V_{DD}$ ), threshold voltage ( $V_{th}$ ), transistor channel length ( $L_{min}$ ), transistor width versus channel length ( $W_{min}/L_{min}$ ), PMOS to NMOS width ratio ( $W_p/W_n$ ), diffusion length ( $L_{diff}$ ), parasitic capacitance ( $C_{pi}$ ), fanout, end of logic chain capacitive load ( $C_{load}$ ), current model (i(t)), collection time constant ( $t_\beta$ ,  $\tau$ ), ion-track establishment ( $t_\alpha$ ), and transistor type (PMOS, NMOS).

#### 5 Simulation

To determine  $Q_{crit}$  and the effects that each of the parameters have on it, we used HSPICE. We used four predictive technology models (22, 32, 45, and 65nm) [23, 33]. Additionally, we considered minor changes to the models, such as  $V_{th}$  variation, using methods described in [9]. Measurements of  $Q_{crit}$  were made using the optimization (OPTIMIZE) function from HSPICE for the cells listed in table 1. We define  $Q_{crit}$  to be the point where the output signal reaches  $V = 0.5 \cdot V_{DD}$  [32]. The test and calibration circuit is shown in figure 2.

Determination of effect estimates were made using the folded over PB design. Parameters with numerical values are varied by  $\pm 10\%$  (e.g. if  $V_{DD}$  has a base value of 1.0v, then the high value = 1.1v and the low value = 0.9v). The other parameters, such as transistor type, are

varied according to description, rather than numerical variation (e.g. high value = PMOS, low value = NMOS).  $Q_{crit}$  is recorded for each trial and an estimate of effects is calculated. Base parameter values were based on relevant related works discussed in section 4, the ITRS roadmap [26], and other sources such as [2, 28, 29].



**Figure 2.** In (a) we see the general model for injecting current pulses. In (b) we see the model for injecting current into a chain of INV cells with capacitive loads generated using fanout. The value of the final capacitor in (b) is  $C_{load}$ .

## 6 Results and Analysis

Results from our screening results are presented in this section.

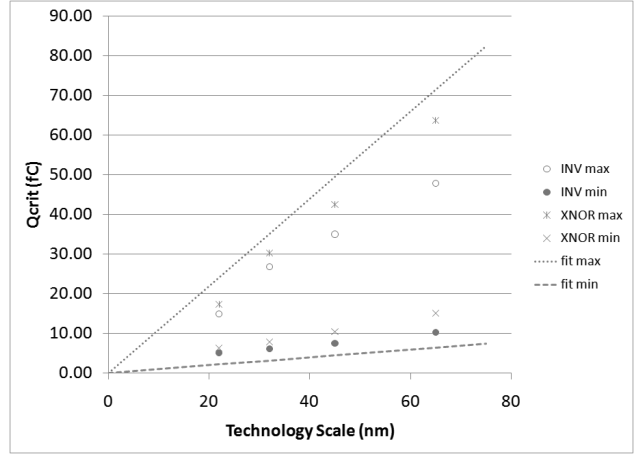
A summary of the rankings are given in table 1. The final column (O) represents no single parameter's rankings, but does represent higher order factors. A rank of 1 indicates the most significant effect on  $Q_{crit}$  and a rank of 15 represents the least significant effect on  $Q_{crit}$ .

In figure 3 the range of  $Q_{crit}$  values that can be obtained from all cells or even within a single cell can vary by large amounts, even within a single technology. In the figure, the upper bound is determined by setting all parameter variations to their high values and vice-versa for the lower bounds, see section 5. Using the SER equation from [27],

$$SER \propto F \times A \times \exp\left(-\frac{Q_{crit}}{Q_s}\right), \quad (4)$$

we find that the ratio of SER for the minimum  $Q_{crit}$  and maximum tends to increase rapidly as  $Q_s \rightarrow 0$ . Here  $Q_s$  is the collection efficiency of the device,  $F$  is particle flux, and  $A$  is critical area. For example, in the 65nm case the maximum and minimum values for  $Q_{crit}$  are around 65fC and 10fC, respectively. With a large  $Q_s$  the ratio of  $SER_{max}$  to  $SER_{min}$  is on the order of 10-100. With a very small  $Q_s$ ,

however, the ratio of  $SER_{max}$  to  $SER_{min}$  can be greater than  $10^{20}$ .



**Figure 3.** In this figure we see the range of  $Q_{crit}$  for each of the four technology scales examined based on the limited cells examined. The upper dotted and lower dashed lines represent the upper and lower bounds for  $Q_{crit}$  respectively.

To determine whether any two-parameter interactions have a significant effect on  $Q_{crit}$ , we examined several of the cells in more detail. For example, in figure 4 we see a normal probability plot for  $Q_{crit}$  effects with the INV cell. There are three regions of interest, indicated by the straight lines. The upper most and right most region is where the most significant effects are indicated. The middle and left-lower most regions then indicate effects of secondary and tertiary significance. We are, generally, only concerned with the primary and secondary effects.

The effects of interest are generally main, single factor, effects. Of the 30 unique 1-parameter or 2-parameter effect estimates<sup>1</sup> only 6, in general, have a primary effect on  $Q_{crit}$ :  $V_{DD}$ (E), transistor type (N),  $V_{th}$ (F),  $W_{min}/L_{min}$ (B), injection current model  $i(t)$  (J), and  $C_{pi}$ (G). There are an additional 6 one and two parameter effects of secondary, but notable, significance, in order of effect: current model fall time (M), temperature (K),  $V_{DD}$  and transistor type (EN), fanout (I),  $V_{th}$  and transistor type (FN), and  $W_p/W_n$ (C). The 2-parameter effects of secondary significance:  $V_{DD}$ +type,  $V_{DD}$ +  $i(t)$  (or  $W_{min}/L_{min}$ +fan out),  $W_{min}/L_{min}$ + type, type +  $i(t)$  (or  $V_{DD}$ + temp),  $W_{min}/L_{min}$ +  $V_{DD}$ , and  $V_{th}$ + fan out. Most other 1, and 2-parameter effects are considered to be minor or negli-

<sup>1</sup>Due to the aliasing structure of the experiment design, many 2-parameter estimates are aliased with one another and measure 15 unique effects rather than 91 two-parameter one might expect without aliasing.

scale		L	W	n/p	dif	vdd	vth	cpi	cl	fan	i(t)	tmp	tri	tfa	mos	
(nm)	cell	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O
22	AOI21	15	4	10	11	2	3	6	14	9	5	7	13	8	1	12
22	INV	14	4	10	11	1	3	6	15	9	5	8	13	7	2	12
22	NAND2	13	3	8	11	1	5	4	15	10	6	7	12	9	2	14
22	NAND3	12	4	7	11	1	5	3	15	10	6	8	13	9	2	14
22	NAND4	11	2	6	12	1	4	3	15	9	5	8	13	10	7	14
22	NOR2	11	3	6	12	1	4	8	15	7	5	10	13	9	2	14
22	NOR3	12	3	6	11	1	4	8	15	7	5	9	14	10	2	13
22	NOR4	12	3	6	11	1	4	8	15	7	5	9	14	10	2	13
22	OAI21	15	4	11	10	2	3	5	14	9	6	7	12	8	1	13
22	XNOR2	7	2	4	12	1	5	8	15	3	6	10	14	11	9	13
22	XOR2	10	2	4	12	1	3	8	15	6	5	9	13	11	7	14
32	AOI21	11	3	10	12	2	4	8	15	7	5	9	13	6	1	14
32	INV	11	3	10	12	2	4	8	15	7	5	9	13	6	1	14
32	NAND2	11	3	10	12	2	5	6	15	8	4	9	14	7	1	13
32	NAND3	10	3	9	12	2	5	6	15	8	4	11	14	7	1	13
32	NAND4	8	3	7	12	1	5	6	15	9	4	11	13	10	2	14
32	NOR2	9	3	7	12	2	4	11	15	6	5	10	14	8	1	13
32	NOR3	9	3	7	12	2	5	11	15	6	4	10	14	8	1	13
32	NOR4	8	3	7	12	2	5	11	15	6	4	10	14	9	1	13
32	OAI21	10	3	12	11	2	4	7	15	8	5	9	14	6	1	13
32	XNOR2	7	3	6	12	1	5	10	14	4	8	11	13	9	2	15
32	XOR2	7	3	8	12	1	5	10	15	6	4	11	14	9	2	13
45	AOI21	8	3	10	12	2	5	11	15	6	4	9	13	7	1	14
45	INV	10	3	8	12	2	5	11	15	6	4	9	13	7	1	14
45	NAND2	9	3	10	12	2	5	8	15	6	4	11	14	7	1	13
45	NAND3	7	3	8	12	2	5	9	15	6	4	11	14	10	1	13
45	NAND4	5	3	8	12	1	7	9	15	6	4	11	13	10	2	14
45	NOR2	8	3	7	12	2	6	11	15	4	5	10	13	9	1	14
45	NOR3	6	3	8	12	2	7	11	15	4	5	10	14	9	1	13
45	NOR4	6	3	7	11	2	8	12	15	4	5	10	14	9	1	13
45	OAI21	10	3	12	11	2	5	8	15	7	4	9	14	6	1	13
45	XNOR2	5	3	6	12	1	8	11	15	4	7	10	13	9	2	14
45	XOR2	5	3	7	12	1	8	11	15	4	6	10	14	9	2	13
65	AOI21	7	3	9	12	2	6	11	15	4	5	10	13	8	1	14
65	INV	8	3	9	12	2	6	11	15	5	4	10	13	7	1	14
65	NAND2	7	3	9	12	2	6	11	15	5	4	10	14	8	1	13
65	NAND3	5	3	8	12	1	7	11	15	6	4	10	14	9	2	13
65	NAND4	4	3	8	12	1	7	10	14	5	6	11	15	9	2	13
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65	NOR4	5	3	7	11	2	8	12	15	4	6	10	14	9	1	13
65	OAI21	7	3	12	11	2	5	10	15	6	4	9	14	8	1	13
65	XNOR2	5	3	6	11	1	7	12	14	4	8	10	15	9	2	13
65	XOR2	4	3	6	11	1	8	12	15	5	7	10	14	9	2	13
	avg	8.5	3.0	8.0	11.6	1.6	5.4	9.0	14.9	6.1	5.1	9.6	13.6	8.5	1.8	13.3
	var	8.9	0.2	3.8	0.3	0.3	2.4	6.5	0.1	3.5	1.2	1.2	0.4	1.7	2.8	0.4

**Table 1. Summary of parameter rankings. A rank of 1 indicates the greatest effect and 15 the least.**

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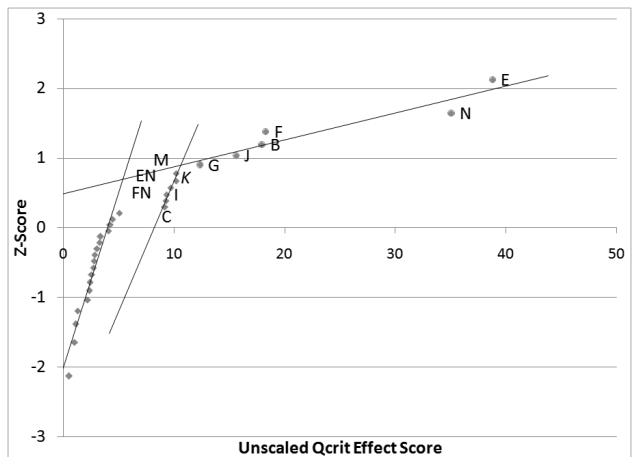
### 6.1 Analysis of Results

Supply voltage and transistor type have the greatest effect on  $Q_{crit}$  of any parameters. As  $V_{DD}$  is linked to technology scaling, more attention should then be spent on dealing with transistor type and other effects. These are followed, in significance, by transistor width, current model, and threshold voltage. Secondary effects then follow, including:  $W_p/W_n$ ,  $t_\beta$ , and channel length.

The rankings combined with the estimated effects support the claim that drive current generally has a greater effect on  $Q_{crit}$  than capacitance [5].

It is also worth noting that the current model does have a significant impact on the measurement of  $Q_{crit}$ . Even with equal charge and pulse width, the difference in the current models is significant enough to alter  $Q_{crit}$  by 10% as seen in figure 1. Further investigation on this matter is warranted due to the significance in effect.

Finally, it is worth noting that the statistical variation in ranking, and in effect, of a few parameters is significant. These include channel length, parasitic capacitance, and



**Figure 4. A normal probability plot for the INV cell at the 22nm technology scale shows three regions of effects, as indicated by the lines.**

$W_p/W_n$ . This demonstrates the need to consider cells and particular technologies individually when calculating SER and designing for SER reduction. For example, we see similar ranking of effects for the AOI21 cell and the INV cell in the 22nm technology, but both differ in a few key areas, such as  $W_{min}/L_{min}$  when compared to the rankings of the XOR2 and XNOR2 cells.

The cost of characterizing every individual cell in large designs is almost certainly too costly, but a summary of parameter impact could be used to improve future designs. For example, a designer may rely upon a table of parameter effect rankings to direct which cells are considered for fault-tolerance, rather than relying upon data for a single cell.

## 7 Conclusion

In this paper we have highlighted the danger of relying upon single estimates of  $Q_{crit}$  in SER estimation and fault-tolerance assessment and have shown that a few key parameters dominate the effect on  $Q_{crit}$  across various cells technology models. We have shown that supply voltage and transistor width are the most important factors. These factors are followed by width, injection current model, threshold voltage and fanout in significance of effect on  $Q_{crit}$ . In the future we intend to show how these results can be automatically integrated into the circuit design process.

## 8 Acknowledgments

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